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Please substitute the following paragraph for th paragraph beginning at line 3:

Next, as shown in Fig. 21, metal wirings 20 to 27 are formed on the silicon wafer 1A; and, as shown in Fig. 22, metal wirings 20 to 27 are formed on the silicon wafer 1B. The metal wirings 20 to 27 are formed, for example, through the processing of: depositing an aluminum alloy film on the silicon oxide film 15 including the insides of the contact holes 16, 17 by the sputtering method, and patterning the aluminum alloy film by the dry etching with the photo resist film served as the mask. The metal wirings 20 to 27 on the silicon wafer 1A and the metal wirings 20 to 27 on the silicon wafer 1B are formed in the same manner with the same photo mask.

IN THE CLAIMS:

1. (Amended) A semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrat ,

wherein a first voltage is applied to said plurality of first MOS transistors,

wherein a second voltage smaller than said first voltage is applied to said plurality of second MOS transistors,

wherein a gate length of a first gate electrode of said plurality of first MOS transistors is larger than a gate length of a second gate electrode of said plurality of second MOS transistors, and

wherein a spacing between said first gate electrode of the first MOS transistors and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a spacing between said second gate electrode and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors.

B1 cont.

2. (Amended) A semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS

transistors in a second area of the principal plane on th semiconductor substrate,

wherein a first voltage is applied to said plurality of first MOS transistors,

wherein a second voltage smaller than said first voltage is applied to said plurality of second MOS transistors,

wherein a gate length of a first gate electrode of said plurality of first MOS transistors is larger than a gate length of a second gate electrode of said plurality of second MOS transistors, and

wherein a spacing between an edge of a first active region in which the first MOS transistors are formed and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a spacing between an edge of a second active region in which the second MOS transistors are formed and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors.

3. (Twice Amended) A semiconductor device according to Claim 1,

wherein said input circuit or said output circuit operates with said first voltage, and

wherein said internal circuit operates with said second voltage.

4. (Twice Amended) A semiconductor device according to Claim 1,

wherein said plurality of first MOS transistors are first voltage withstanding MOS transistors, and

wherein said plurality of second MOS transistors are second voltage withstanding MOS transistors.

5. (Amended) A semiconductor device according to Claim 1,

wherein a gate insulating film thickness of the first MOS transistors is larger than a gate insulating film thickness of the second MOS transistors.

6. (Amended) A semiconductor device according to Claim 1,

wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed.

DF cancel.

7. (Twice Amended) A semiconductor device according to Claim 1,

wherein said plurality of first MOS transistors are p-channel type, and the source of each of said plurality of first MOS transistors is supplied with said first voltage, and

wherein said plurality of second MOS transistors are p-channel type, and the source of each of said plurality of second MOS transistors is supplied with said second voltage.

B10

21. (Amended) A semiconductor device according to Claim 2,

wherein said input circuit or said output circuit operates with said first voltage, and wherein said internal circuit operates with said second voltage.

B11

22. (Amended) A semiconductor device according to Claim 2,

wherein said plurality of first MOS transistors are first voltage withstanding MOS transistors, and

wherein said plurality of second MOS transistors are second voltage withstanding MOS transistors.

B11

23. (Amended) A semiconductor device according to Claim 2,

wherein a gate insulating film thickness of the first MOS transistors is larger than a gate insulating film thickness of the second MOS transistors.

24. (Amended) A semiconductor device according to Claim 2,

wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed.